What is claimed is:

1. A method of forming a bump pad of a flip chip, comprising:

a first step of subjecting a surface of an insulating layer to electroless copper plating to prepare an electroless copper plating layer, which is then coated with a photosensitive material;

a second step of exposing to light and developing the photosensitive material to prepare a resist pattern, which is then pulse plated to form a pulse plating layer;

a third step of subjecting the pulse plating layer to electrolytic copper plating using a direct current, to prepare a direct current plating layer; and

a fourth step of removing the resist pattern prepared at the second step and the electroless copper plating layer prepared at the first step.

2. The method as defined in claim 1, wherein the first step comprises the formation of the electroless copper plating layer by subjecting the surface of the insulating layer to electroless copper plating, and the coating of the photosensitive material on the electroless copper plating layer.

3. The method as defined in claim 2, wherein the photosensitive material coated on the electroless copper plating layer is 20 μm thick.

4. The method as defined in claim 2, wherein the photosensitive material coated on the electroless copper plating layer is a dry film.

5. The method as defined in claim 1, wherein the second step comprises the formation of the resist pattern through exposure to light and development of the photosensitive material, and the formation of the pulse plating layer by subjecting the resist pattern to electrolytic pulse plating.

6. The method as defined in claim 5, wherein the pulse plating layer is 5-10 μm thick.

7. A structure of a bump pad of a flip chip, comprising:

a thin electroless copper plating layer having a predetermined thickness and patterned on an insulating layer;

an electroless layer having a predetermined thickness and formed on the thin electroless copper plating layer; and

an electrolytic layer having a predetermined thickness and formed on the electroless layer.

8. The structure as defined in claim 7, wherein the electroless layer and the electrolytic layer are total 20 μm thick.

9. The structure as defined in claim 7, wherein the electrolytic layer is 5-10 μm thick.